**ECEN-607: Advanced Analog IC Design**

**Assignment #2:**

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Due: 02/06/2025

Instructor: Jose Silva-Martinez

Design at transistor level a two-stage amplifier; use the following specifications:

VDD = 1.8 V

VSS = 0 V

Gain > 40 dB

Employ loop compensation; phase margin > 450

GBW > 4 MHz

Load Capacitor = 10 pF

1. Show amplifier’s functionality. Simulate the amplifier and plot both magnitude and phase response. Report screen shots.

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1. Implement a capacitive amplifier with an inverting gain of 6dB, β=1/3; minimum capacitor used in the amplifier must be ≥100fF. You may need to connect a large resistor (>1Mohm) in parallel with the feedback capacitor; why? a. Plot the loop gain; simulate the amplifier and report both magnitude and phase response. b. Plot the step response for an input step of 0 to 100mV variation. Report the 1% setting time and value of the settling error. Ideal output voltage variation should be -200mV. c. Comment on the results.

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1. Repeat ii) for the case of an inverting amplifier with gain=12dB; evidently the feedback factor is different now. For the transient simulation, reduce the size of the input step to 0 50mV.

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